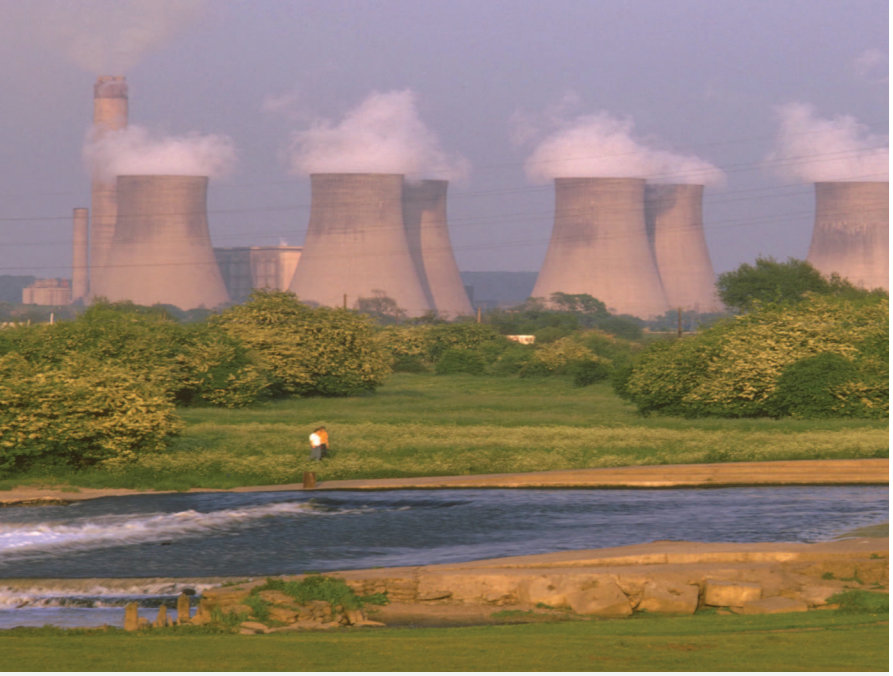


National Aeronautics and Space Administration

technology solution

Electrical and Electronics

Self-Scrubbing Technology for Reconfigurable Rad-Hard Memory Arrays

Novel field programmable gate array technology for single event upset detection and mitigation of radiation effects

NASA's Langley Research Center has developed a firmware approach to mitigating single event upsets (SEUs) in radiation-tolerant field programmable gate arrays (FPGAs), including configuration memory, clock management, and configuration logic. Since this technology can be implemented within an FPGA, there is no need for the additional external hardware currently required for SEU mitigation, thus lowering cost, weight, and power; decreasing complexity; and improving reliability. NASA Langley has developed the technology for high-performance spacebased computing applications. The technology has been tested and will be used on an instrument on NASA's Mars Science Laboratory rover, scheduled for launch in 2009.

BENEFITS

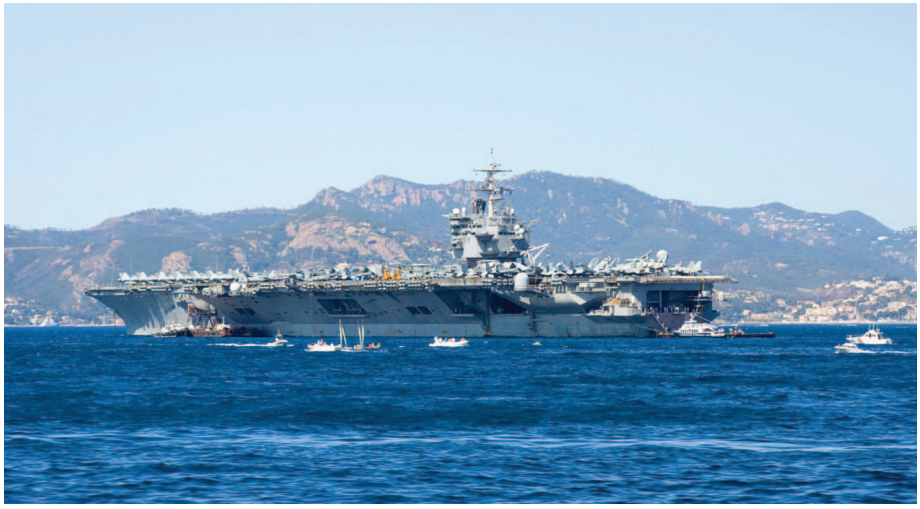
- Improves system reliability
- Increases data accessibility, including:
  -- increased resolution
  -- improved data quality
  -- larger capacity for raw or processed data
- Overcomes errors (hardware and/or software) that are detected after launch
- Reduces mission risk due to memory failure
- Eliminates need for external scrubbing and monitoring hardware, thereby reducing:
  -- cost
  -- size
  -- development time
- Allows use of standard hardware on multiple varied missions (less cost)

THE TECHNOLOGY

NASA developed the technology to meet the needs for on-board satellite data processing for future missions. The continuing trends toward ever-increasing resolution, improved data quality, and additional capacity for raw and/or processed data will necessitate the use of larger on-board memories, which must be made radiation tolerant. This technology is a firmware approach to radiation-tolerant memory, suitable for both GEO and LEO missions.

Memory cells in FPGAs are susceptible to SEUs. It is important to correct configuration memory upset as quickly as possible. NASA has used an approach of refreshing the configuration memory cells at regular intervals. The configuration bit stream is stored in memory and upon power-on, the FPGA loads its configuration from memory. The memory refresh controller is implemented internally in the FPGA. The correction of SEUs in configuration logic requires initial detection of a failure in configuration logic, which has also been developed and incorporated as part of this technology.

In addition to detecting SEUs, the technology implements a scrubbing strategy where the memory contents are read sequentially and when an error is detected, the memory is updated with correct data.



Aircraft carrier

APPLICATIONS

The technology has several potential applications:

- Aerospace high-performance space-based computing for low earth orbit
  (LEO) and geosynchronous earth orbit (GEO) missions
  -- real-time data processing
  -- adaptive/reconfigurable computing
  -- memory-intensive systems
- Nuclear radiation-tolerant memory for
  -- facilities/plants

  --powered craft: aircraft carriers, submarines
- Defense protection from warfare radiation sources

PUBLICATIONS

Patent No: 7,590,904; 7,647,543

More Information

National Aeronautics and Space Administration

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NP-2014-09-1186-HQ

NASA's Technology Transfer Program pursues the widest possible applications of agency technology to benefit US citizens. Through partnerships and licensing agreements with industry, the program ensures that NASA's investments in pioneering research find secondary uses that benefit the economy, create jobs, and improve quality of life.

LAR-17257-1, LAR-17268-1